WHAT IS CLAIMED:

1. A system on a chip comprising:

a first power plane for powering a core logic portion of the system on a chip;

a second power plane for powering selected analog circuitry of the system on a chip;

clock generation circuitry for generating clocks for clocking operations of selected circuits of the system on the chip in response to a signal generated by an oscillator; and

power control circuitry operable to:

in a first mode, switch-off power to the first and second power planes, the oscillator being enabled; and

in a second mode, disable the clock generation circuitry and switch power to the first and second power planes, the oscillator being enabled.

2. The system on a chip of Claim 1 wherein the selected analog circuitry comprises a phase-locked loop circuit.

3. The system on a chip of Claim 1 wherein the selected analog circuitry comprises and analog to digital converter.

4. The system on a chip of Claim 1 wherein the core logic comprises a microprocessor.

5. The system on a chip of Claim 1 wherein the core logic comprises a digital signal processor.

6. The system on a chip of Claim 1 and further comprising a third power plane for powering a pulse width modulation engine, the power control circuitry switching-off power to the third power plane in the first mode and switching power to the third power plane in the second mode.

7. The system on a chip of Claim 4 wherein the control circuitry is further operable in a pause mode to pause execution instructions by the microprocessor, the power control circuitry switching power to the first and second power planes and the oscillator enabled during the pause mode.

8. The system on a chip of Claim 1 wherein the power control circuitry is operable to generate a signal for transmission to an external switch for switching-off power to the selected ones of the power planes in the first mode.

9. A method of power control in a system on a chip including core logic powered by a first power plane, analog circuitry powered by a second power plane and clock generation circuitry for generating clocks for operating selected circuitry of the core logic in response to a clock signal generated by an oscillator comprising the steps of:

during a normal mode of operation, selectively powering the first and second power planes and running the oscillator;

during a super stand-by mode, selectively terminating power to the first and second power planes and running the oscillator; and

during a stand-by mode, selectively powering the first and second power planes, disabling the clock generation circuitry and running the oscillator.

10. The method of power control of Claim 9 and further comprising the steps of:

entering the super-standby mode by setting a bit with a processor forming a portion of the core logic; and

exiting the super-standby mode in response to a wake-up signal received from an external source.

11. The method of power control of Claim 9 and further comprising the steps of:

entering the stand-by mode in response to a bit set with a processor forming a portion of the core logic; and

exiting the stand-by mode in response to a signal received from an external source.

12. The method of power control of Claim 9 wherein the core logic comprises a microprocessor and further comprising the steps of:

pausing execution of instructions by the microprocessor during a pause mode; and

exiting the pause mode in response to an interrupt to the microprocessor.

13. The method of Claim 9 wherein the clock generation circuitry comprises a phase-locked loop and said steps of enabling and disabling comprise the steps of powering-up and powering-down the phase-locked loop.

14. The method of Claim 10 wherein said step of entering the super stand-by mode comprises the substeps of:

generating a signal within the system on a chip; and

disabling an external power supply supplying the first and second power planes in response to the signal generated within the system on a chip.

15. A system on a chip comprising:

a microprocessor operating from a first bus and operating in response to a microprocessor clock;

a digital signal processor operating from the first bus and operating in response to a DSP clock;

a first power plane for providing power to said microprocessor and said digital signal processor;

analog circuitry operating from a second bus coupled to the first bus by a bridge;

a second power plane for providing power to said analog circuitry; and

power control circuitry operable in a first stand-by mode decouple power from said first and second power planes and in a second stand-by mode to terminate generation said microprocessor and DSP clocks while maintaining power to said first and second power planes.

16. The system on a chip of Claim 15 and further comprising a pulse width modulator operating from said second bus and a third power plane for powering said pulse width modulator, said power control circuitry further operable to decouple power from said third power plane in the first stand-by mode.

17. The system on a chip of Claim 15 and further comprising a phase-locked loop operating from said second bus for generating said microprocessor and DSP clocks, said power control circuitry operable to power-down said phase-locked loop in the second stand-by mode.

18. The system on a chip of Claim 15 wherein said microprocessor is operable to set a bit and enter a pause mode and exit said pause mode in response to an interrupt received on said first bus.

19. The system on a chip of Claim 15 wherein the analog circuitry comprises a phase-locked loop and an analog to digital converter.

20. The system on a chip of Claim 15 and further comprising a pad ring for driving input/output ports to selected circuitry of said system on a chip and a third power plane for powering said pad ring, said power control circuitry operable to decouple power from said third power plane during said first stand-by mode.